**Diagram, schematic

Description automatically generatedCircuit Diagram & Truth Table:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **S0** | **S1** | **i0** | **i1** | **i2** | **i3** | **out1** | **out2** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |

**Code:**

* **Design Module**

module rom(out1,out2,s0,s1,i0,i1,i2,i3);

input s0,s1,i0,i1,i2,i3;

output out1,out2;

wire s0n,s1n,a,b,c,d;

not n1(s0n,s0);

not n2(s1n,s1);

and a1(a,s0n,s1n,i0);

and a2(b,s0n,s1,i1);

and a3(c,s0,s1n,i2);

and a4(d,s0,s1,i3);

or o1(out1,a,b);

or o2(out2,c,d);

endmodule

* **TestBench**

module Baig;

reg s0,s1,i0,i1,i2,i3;

wire out1,out2;

rom r1(out1,out2,s0,s1,i0,i1,i2,i3);

initial

begin

s0=1'b0;s1=1'b0;i0=1'b0;i1=1'b0;i2=1'b0;i3=1'b0;

#20

s0=1'b0;s1=1'b0;i0=1'b0;i1=1'b0;i2=1'b0;i3=1'b1;

#20

s0=1'b0;s1=1'b1;i0=1'b0;i1=1'b0;i2=1'b1;i3=1'b0;

#20

s0=1'b0;s1=1'b1;i0=1'b0;i1=1'b0;i2=1'b1;i3=1'b1;

#20

s0=1'b1;s1=1'b0;i0=1'b0;i1=1'b1;i2=1'b0;i3=1'b0;

#20

s0=1'b1;s1=1'b0;i0=1'b0;i1=1'b1;i2=1'b0;i3=1'b1;

#20

s0=1'b1;s1=1'b1;i0=1'b0;i1=1'b1;i2=1'b1;i3=1'b0;

#20

s0=1'b1;s1=1'b1;i0=1'b0;i1=1'b1;i2=1'b1;i3=1'b1;

#20

$finish;

end

endmodule

**Output:**

Graphical user interface, application, table

Description automatically generated